Amendments to the Claims:

Please amend claims 1-16, 23-25, and 27-29 as follows. Please cancel claim 24 as follows. Please add new claims 30-32 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) ~~An internal voltage generating circuit of a~~ A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related ~~according~~ to a number of [[data]] bits being processed by the semiconductor device, wherein the control signal is ~~inactivated~~ activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of [[data]] bits being processed by the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, the internal voltage generating circuit comprising:

a comparing circuit ~~enabled by being provided an external power voltage as a power voltage when the control signal is inactivated, and~~ for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated;

a driving signal control circuit ~~enabled when the control signal is activated, and~~ for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving [[the]] an external power voltage and ~~making the internal voltage have the reference voltage level~~ generating the internal voltage in response to the driving signal~~, and making the internal voltage have the external power voltage~~

~~level when the driving signal is inactivated~~.

2. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the driving signal control circuit includes an NMOS transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied, and a source connected to a ground voltage.

3. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the internal voltage driving circuit includes a PMOS transistor which has a source to which the external power voltage is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage, wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage level when the driving signal is inactivated.

4. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the comparing circuit includes:

a comparator connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated.

5. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the comparing circuit includes:

a comparator connected between a first node and a second node and comparing the reference voltage to the internal voltage to generate the driving signal;

a first switching circuit connected between the external power voltage and the first node

and cutting off the external power voltage applied to the comparator when the control signal is activated; and

a second switching circuit connected between the second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated.

6. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the comparing circuit includes:

a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated.

7. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the ~~control~~ input signal ~~generating circuit activates or inactivates the control signal using~~ is generated using a fuse ~~option~~.

8. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the ~~control~~ input signal ~~generating circuit activates or inactivates the control signal~~ is generated using ~~a bonding~~ an external pad ~~option~~.

9. (Currently Amended) The ~~circuit~~ device of claim 1, wherein the input ~~control~~ signal is ~~generating circuit activates or inactivates the control signal by receiving~~ a mode setting signal comprising a plurality of mode setting bits ~~together with a mode setting command~~.

10. (Currently Amended) ~~An internal voltage generating circuit of a~~ A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related ~~according~~ to a number of [[data]] bits being processed by the semiconductor

device, wherein the control signal is ~~inactivated~~ activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of [[data]] bits being processed by the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, the internal voltage generating circuit comprising:

a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal;

a switching circuit for transmitting the comparing signal as a driving signal when the control signal is inactivated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

11. (Currently Amended) The ~~circuit~~ device of claim 10, wherein the driving signal control circuit includes an NMOS transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied, and a source connected to a ground voltage.

12. (Currently Amended) The ~~circuit~~ device of claim 10, wherein the internal voltage driving circuit includes a PMOS transistor which has a source to which the external power voltage is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage, wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage level when the driving signal is inactivated.

13. (Currently Amended) The ~~circuit~~ device of claim 10, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated.

14. (Currently Amended) The ~~circuit~~ device of claim 10, wherein the ~~control~~ input signal ~~generating circuit activates or inactivates the control signal using~~ is generated using a fuse ~~option~~.

15. (Currently Amended) The ~~circuit~~ device of claim 10, wherein the ~~control~~ input signal ~~generating circuit activates or inactivates the control signal~~ is generated using ~~a bonding~~ an external pad ~~option~~.

16. (Currently Amended) The ~~circuit~~ device of claim 10, wherein the input ~~control~~ signal is ~~generating circuit activates or inactivates the control signal by receiving~~ a mode setting signal comprising a plurality of mode setting bits ~~together with a mode setting command~~.

17. (Withdrawn) An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a first internal voltage generating circuit for receiving a reference voltage and an internal voltage to turn the internal voltage to a reference voltage level;

a second internal voltage generating circuit for receiving an external power voltage to turn the internal voltage to an external power voltage level;

a first switching circuit for supplying the external power voltage to the first internal voltage generating circuit when the control signal is inactivated; and

a second switching circuit for supplying the external power voltage to the second internal voltage generating circuit when the control signal is activated.

18. (Withdrawn) The circuit of claim 17, wherein the first switching circuit includes a CMOS transmission gate which supplies the external power voltage to the first internal voltage generating circuit when the control signal is inactivated.

19. (Withdrawn) The circuit of claim 17, whereint the switching circuit includes a CMOS transmission gate which supplies the external power voltage to the second internal voltage generating circuit when the control signal is inactivated.

20. (Withdrawn) The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal using a fuse option.

21. (Withdrawn) The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal using a bonding option.

22. (Withdrawn) The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command.

23. (Currently Amended) ~~An internal voltage generating circuit of a~~ A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related ~~according~~ to a number of [[data]] bits being processed by the semiconductor device, wherein the control signal is ~~inactivated~~ activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of [[data]] bits being processed by the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal and comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated.

24. (Canceled)

25. (Currently Amended) The ~~circuit~~ device of claim 23, wherein the internal voltage generating circuit includes:

a comparing circuit for comparing the reference voltage to the internal voltage to generate a comparing signal;

a switching circuit for transmitting the comparing signal as a driving signal when the control signal is inactivated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

26. (Withdrawn) The circuit of claim 23, wherein the second internal voltage generating circuit:

a first internal voltage generating circuit for receiving the second reference voltage and the second internal voltage to turn the second internal voltage to a second reference voltage level;

a second internal voltage generating circuit for receiving an external power voltage to turn the second internal voltage to an external power voltage level;

a first switching circuit for supplying the external power voltage to the first internal voltage generating circuit when the control signal is inactivated; and

a second switching circuit for supplying the external power voltage to the second internal voltage generating circuit when the control signal is activated.

27. (Currently Amended) The ~~circuit~~ device of claim 23, wherein the ~~control~~ input signal ~~generating circuit activates or inactivates the control signal using~~ is generated using a fuse ~~option~~.

28. (Currently Amended) The ~~circuit~~ device of claim 23, The ~~circuit~~ device of claim 1, wherein the ~~control~~ input signal ~~generating circuit activates or inactivates the control signal~~ is generated using ~~a bonding~~ an external pad ~~option~~.

29. (Currently Amended) The ~~circuit~~ device of claim 23, wherein the input ~~control~~ signal ~~is generating circuit activates or inactivates the control signal by receiving~~ a mode setting signal comprising a plurality of mode setting bits ~~together with a mode setting command~~.

30. (New) The device of claim 9, wherein a value represented by the mode setting bits and a mode setting command are used by the control signal generating circuit to generate the control signal, the value of the mode setting bits corresponding to the number of bits being processed by the semiconductor device.

31. (New) The device of claim 16, wherein a value represented by the mode setting bits and a mode setting command are used by the control signal generating circuit to generate the control signal, the value of the mode setting bits corresponding to the number of bits being processed by the semiconductor device.

32. (New) The device of claim 29, wherein a value represented by the mode setting bits and a mode setting command are used by the control signal generating circuit to generate the control signal, the value of the mode setting bits corresponding to the number of bits being processed by the semiconductor device.